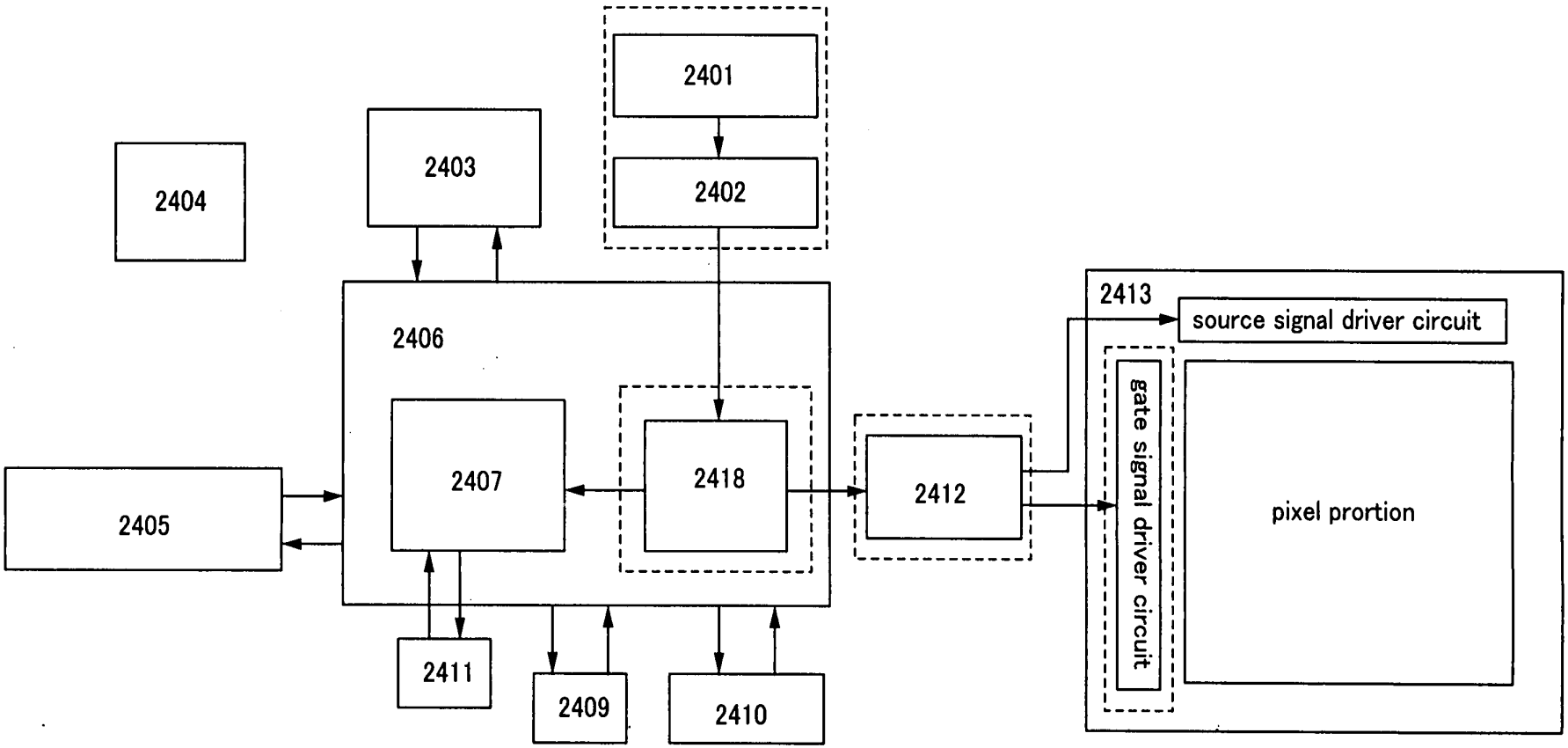

2401
2402
2403
2404
2405
2406
2407
2409
2410
2411
2412
2413
2418
source signal driver circuit
gate signal driver circuit
pixel prortion

Fig. 1

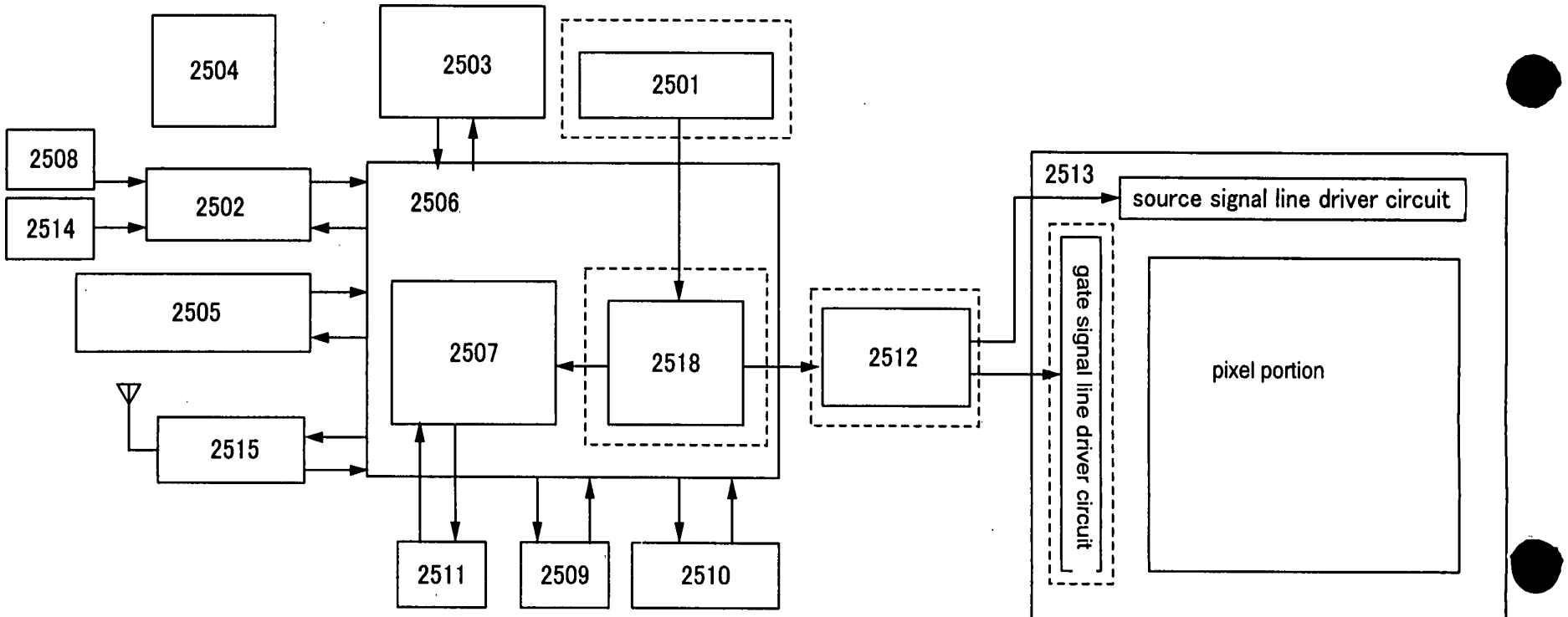

2504
2503
2501
2508
2514
2502
2506
2513
source signal line driver circuit
2505
2507
2518
2512
gate signal line driver circuit
pixel portion
2515
2511
2509
2510

Fig. 2

Fig. 3A

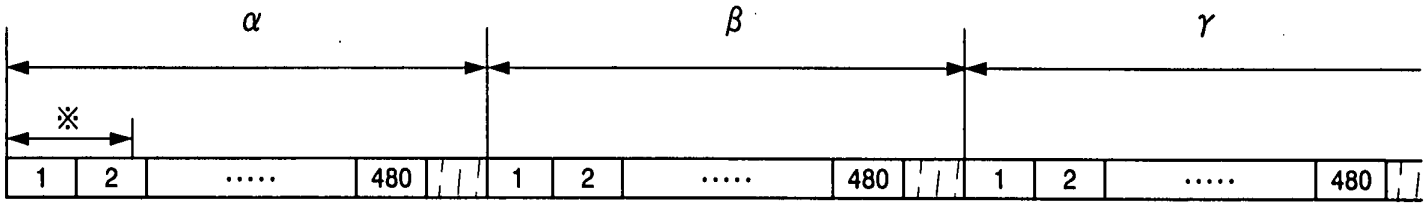
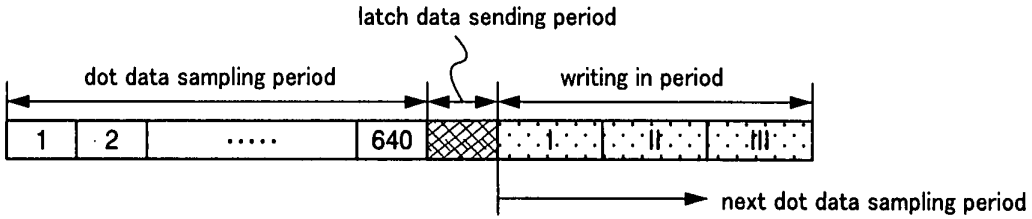

α
β
γ
※
1
2
.....
480
1
2
.....
480
1
2
.....
480

Fig. 3B


latch data sending period
dot data sampling period
writing in period
1
2
.....
640
I
II
III
next dot data sampling period

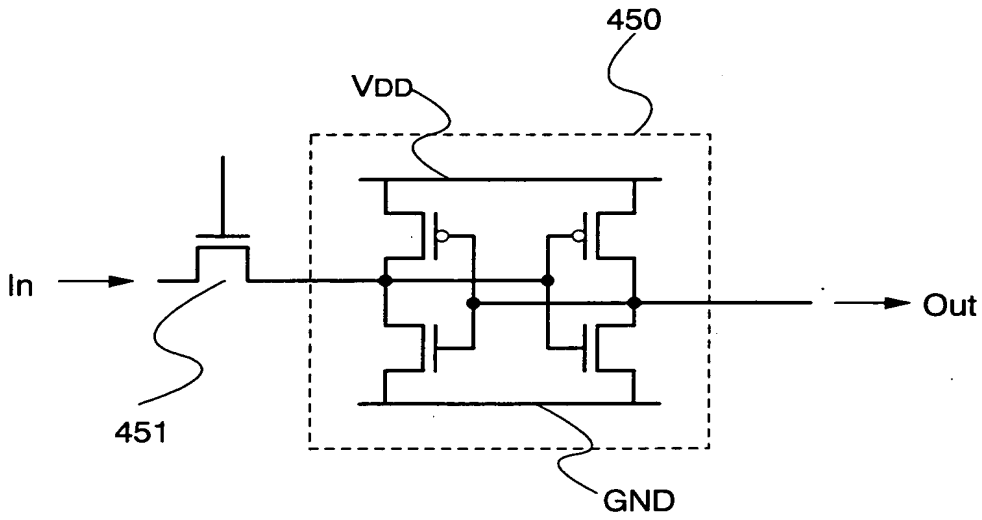


Fig. 4

Padded Redacted

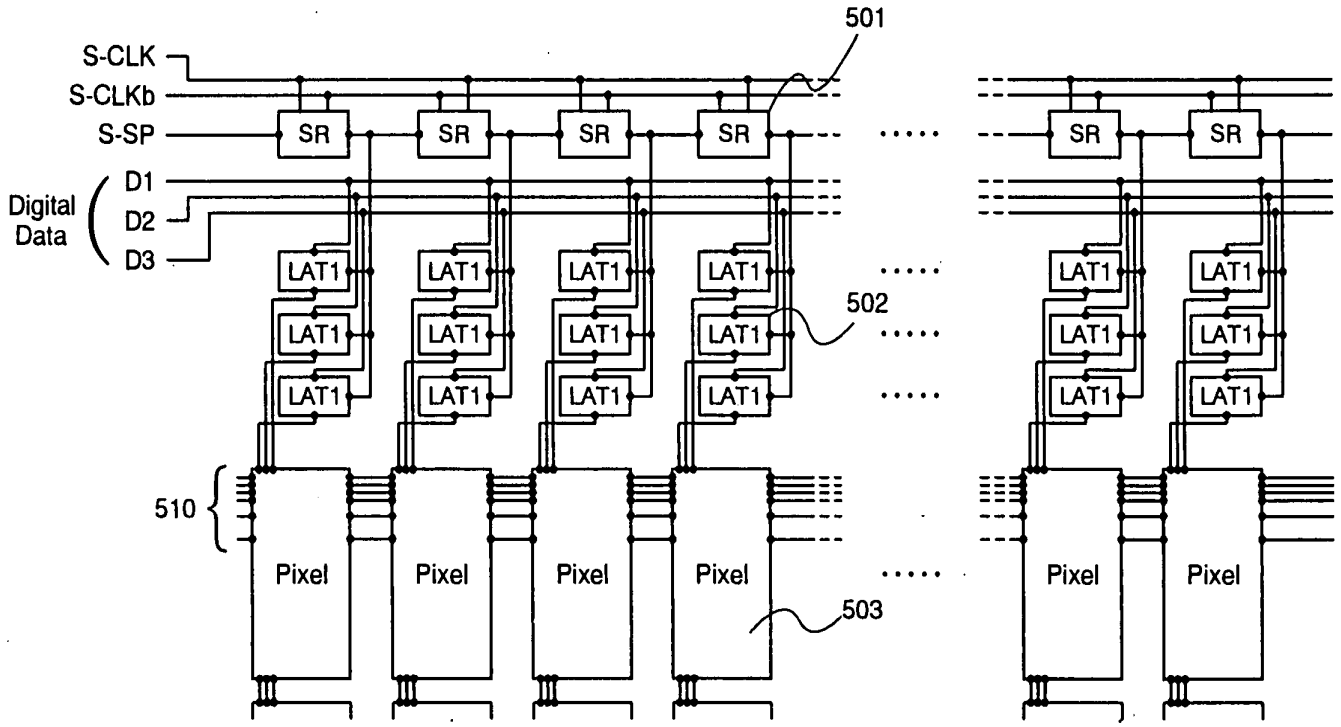


Fig. 5

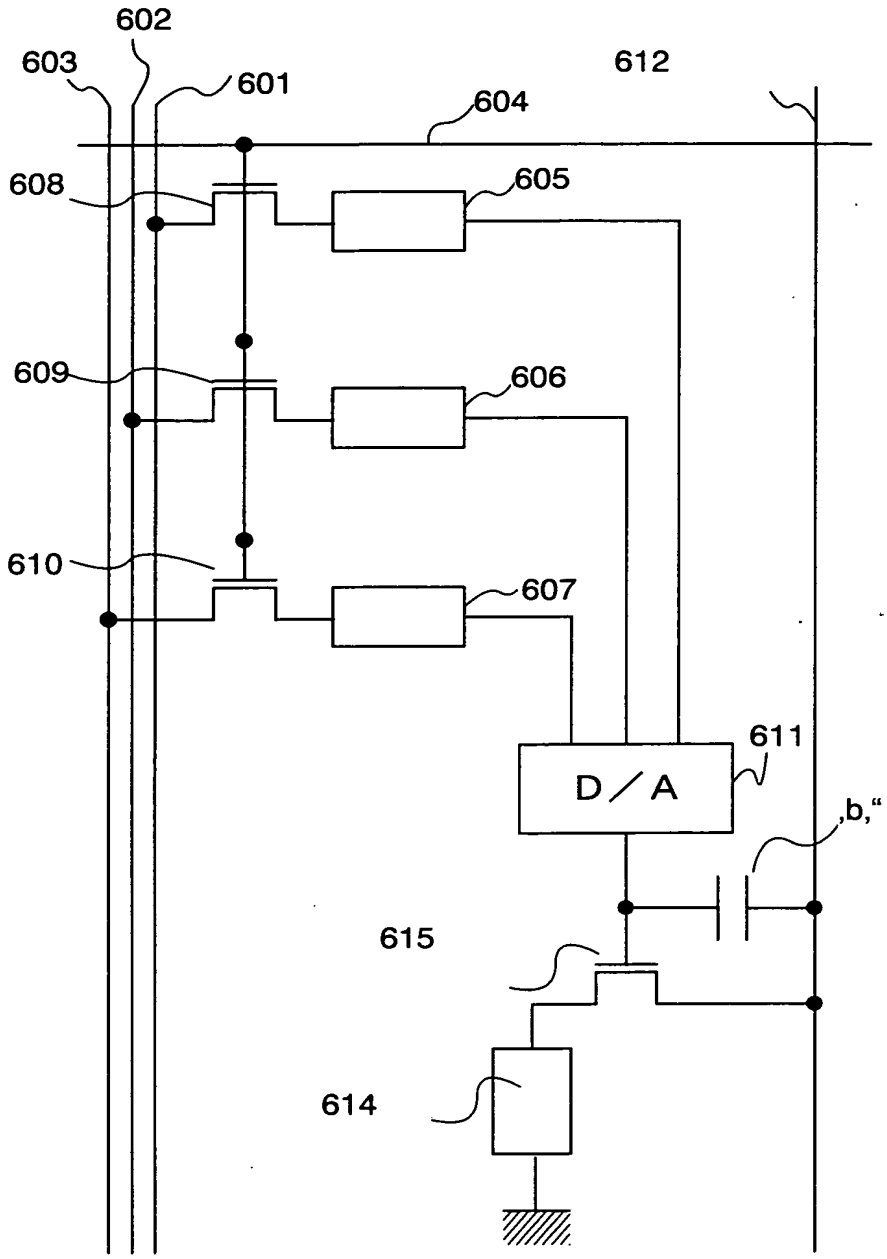


Fig. 6

JP2000-221669

Fig. 7A

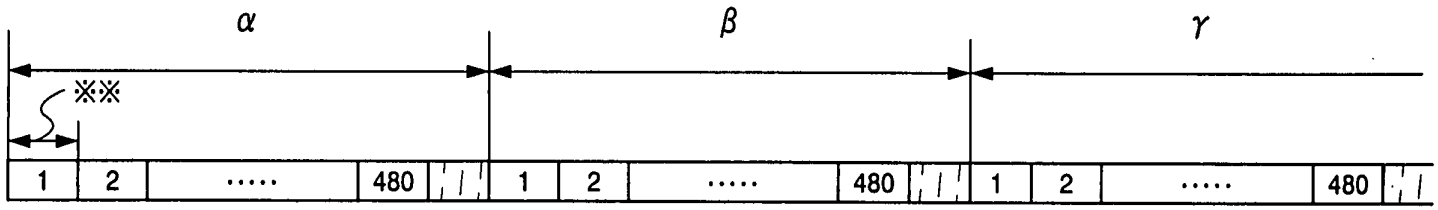
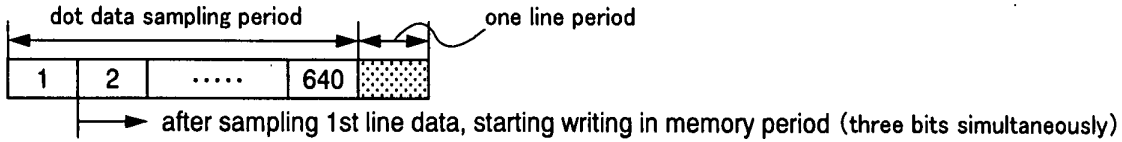


Fig. 7B



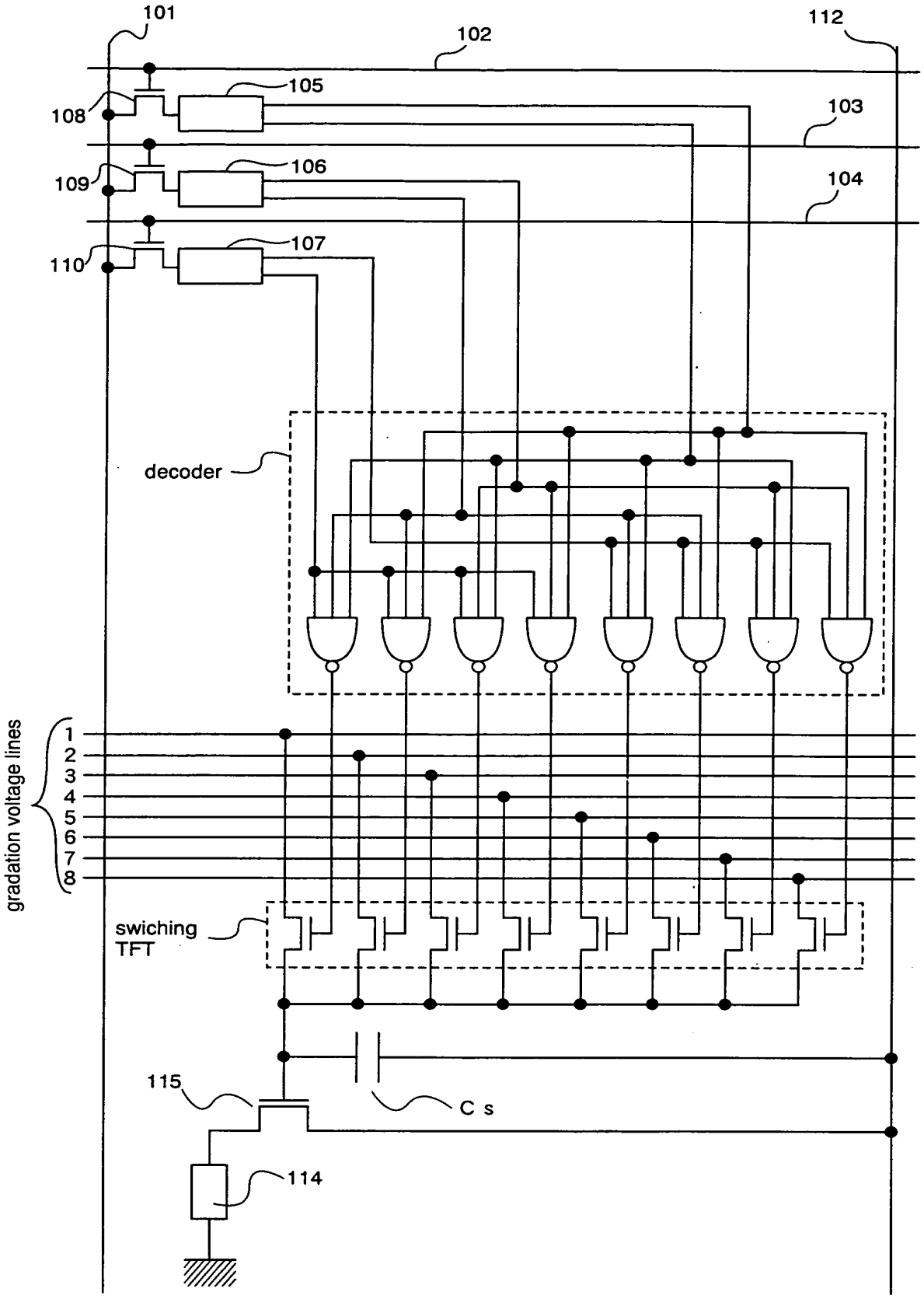

101
102
112
105
108
103
106
109
104
107
110
decoder
gradation voltage lines
1
2
3
4
5
6
7
8
swiching
TFT
115
C s
114

Fig. 8

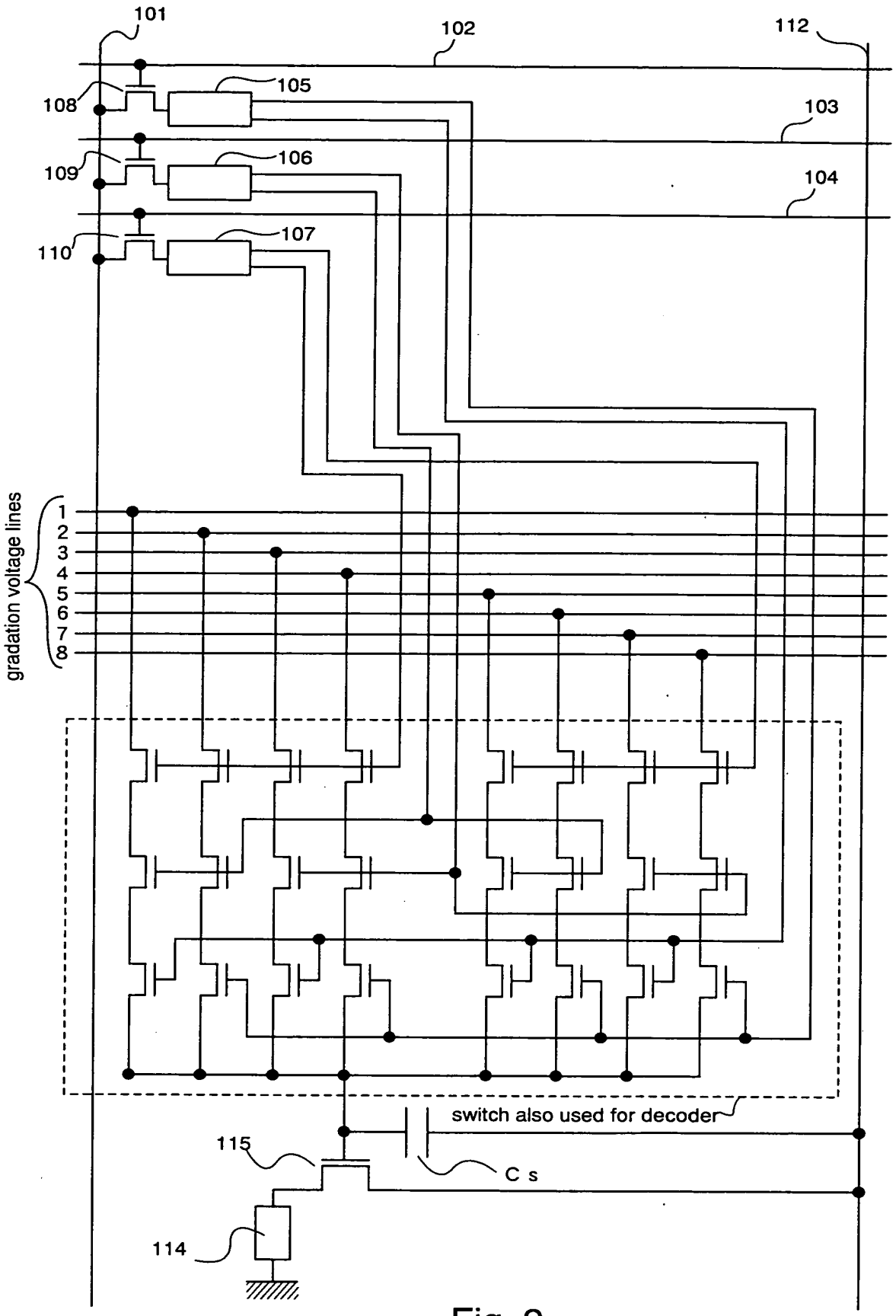

101
102
112
105
108
103
106
109
104
107
110
gradation voltage lines
1
2
3
4
5
6
7
8
switch also used for decoder
115
C s
114

Fig. 9

Fig. 10A

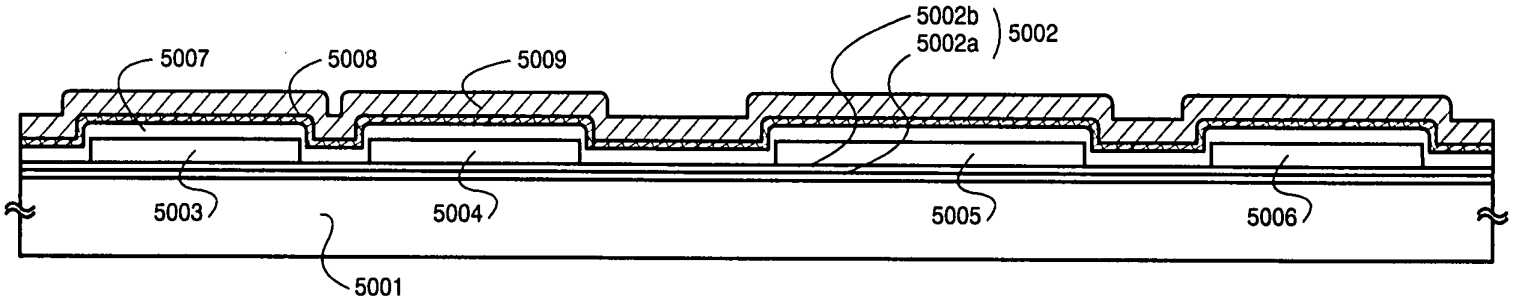


Fig. 10B

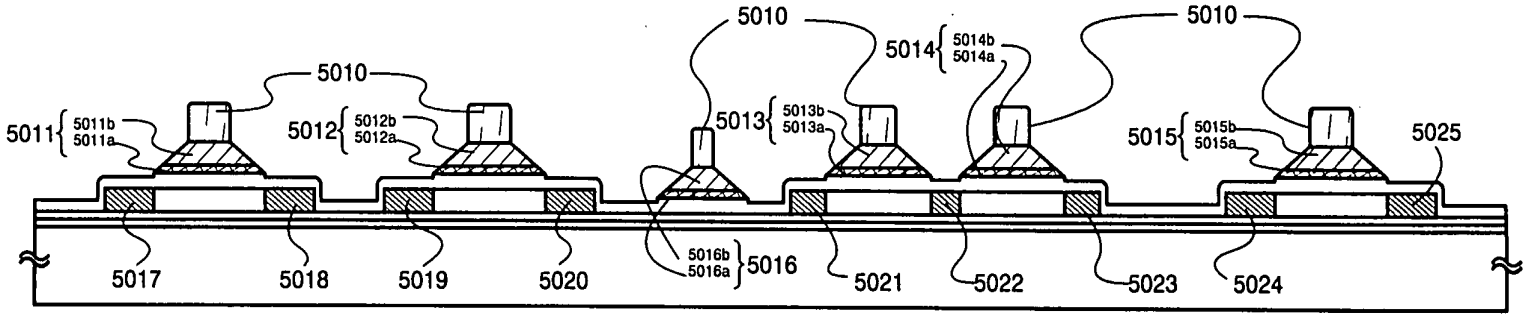


Fig. 10C

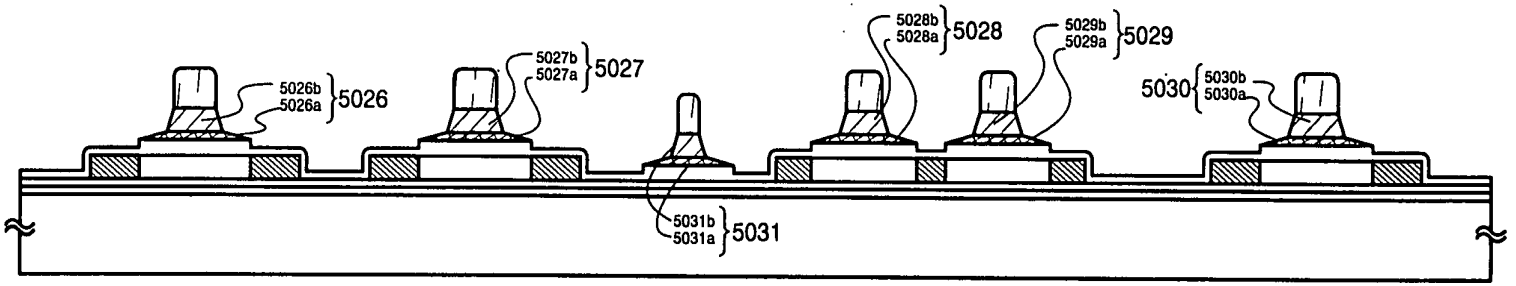


Fig. 11A

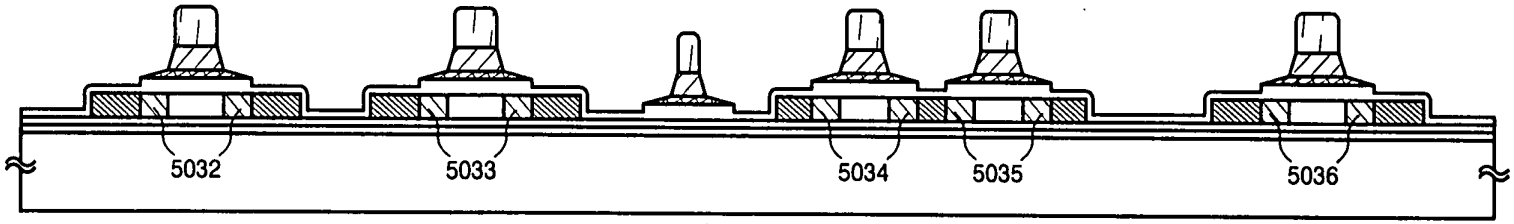


Fig. 11B

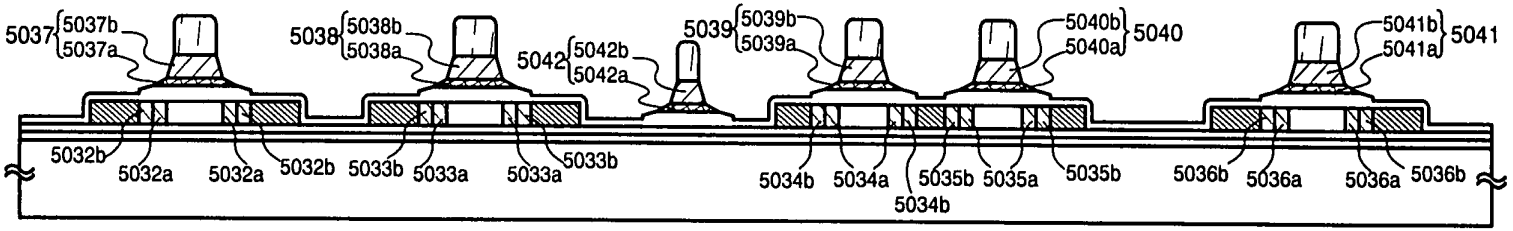


Fig. 11C

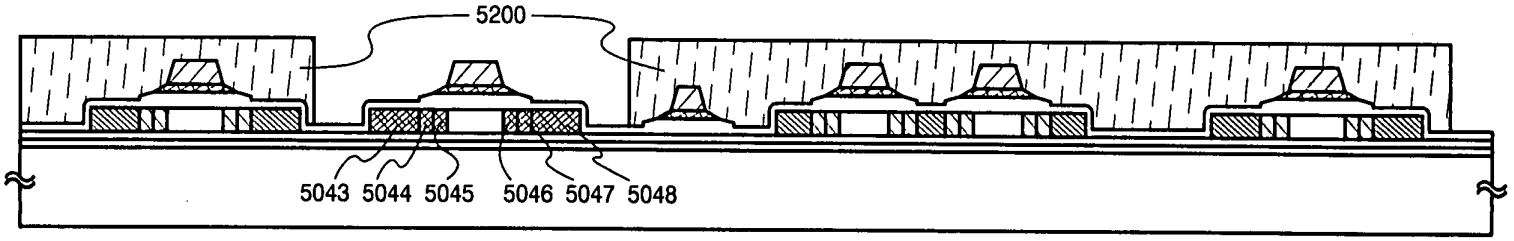


Fig. 12A

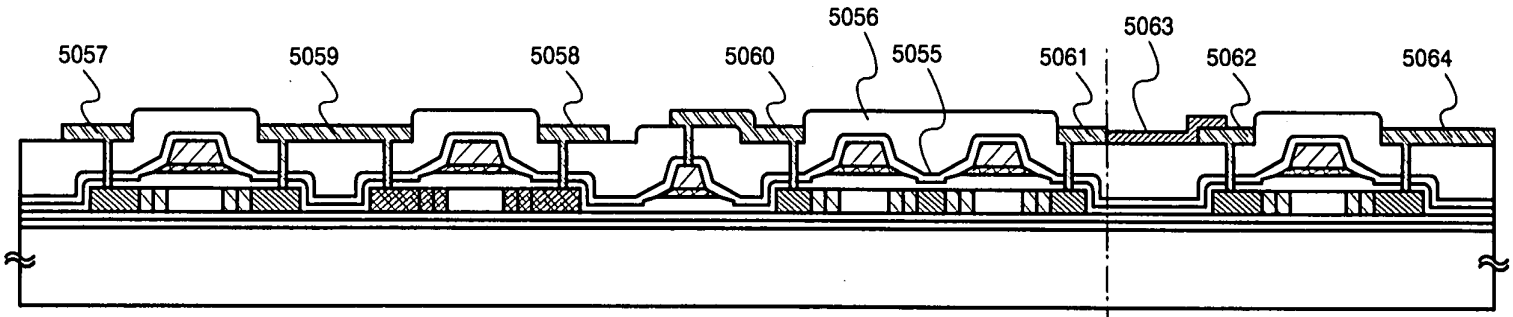
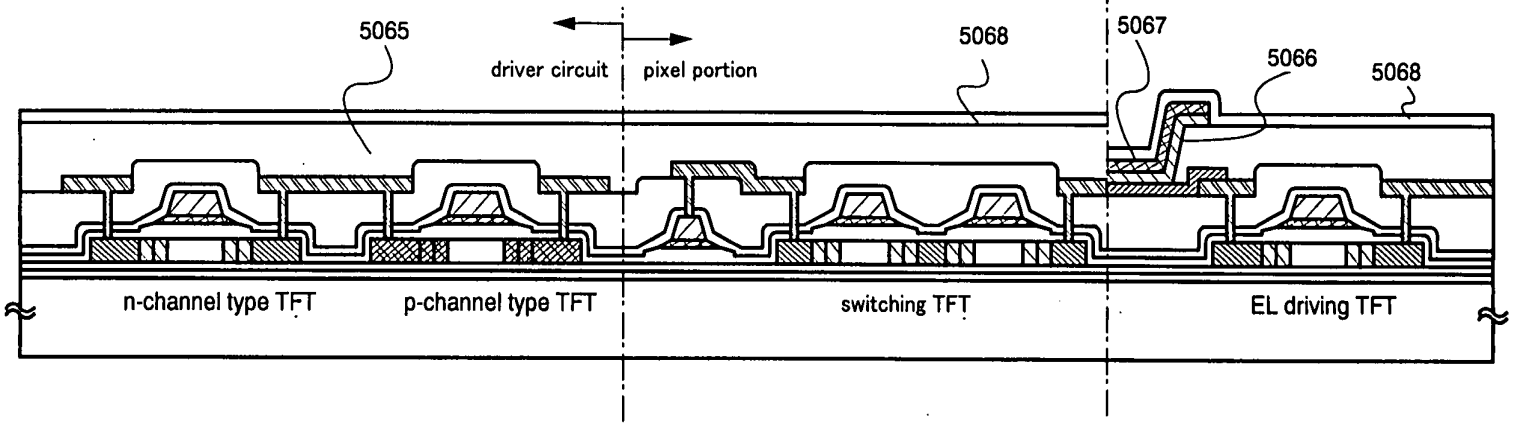


Fig. 12B



T02060 "2660660

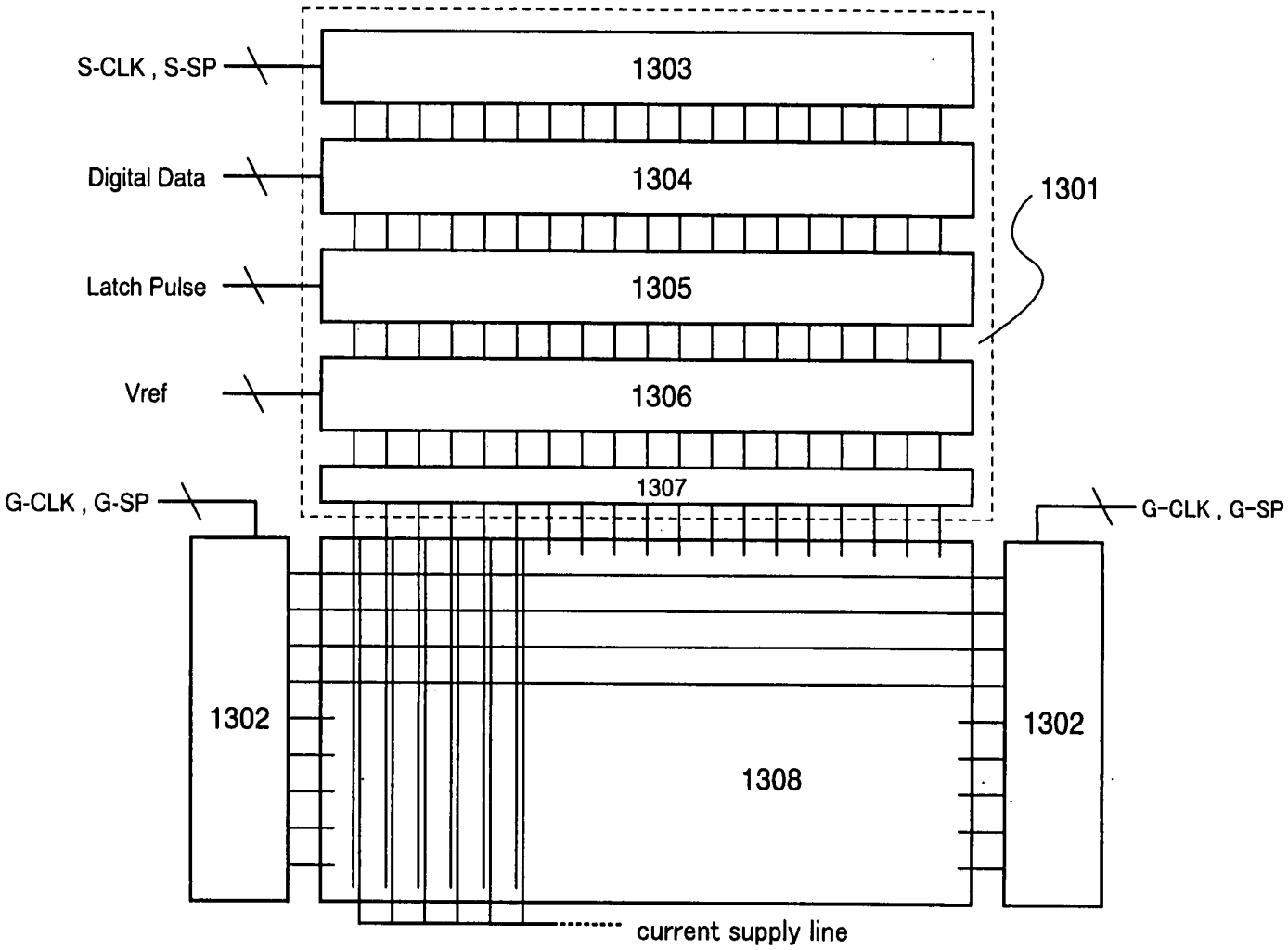


Fig. 13

TO2060 22667660

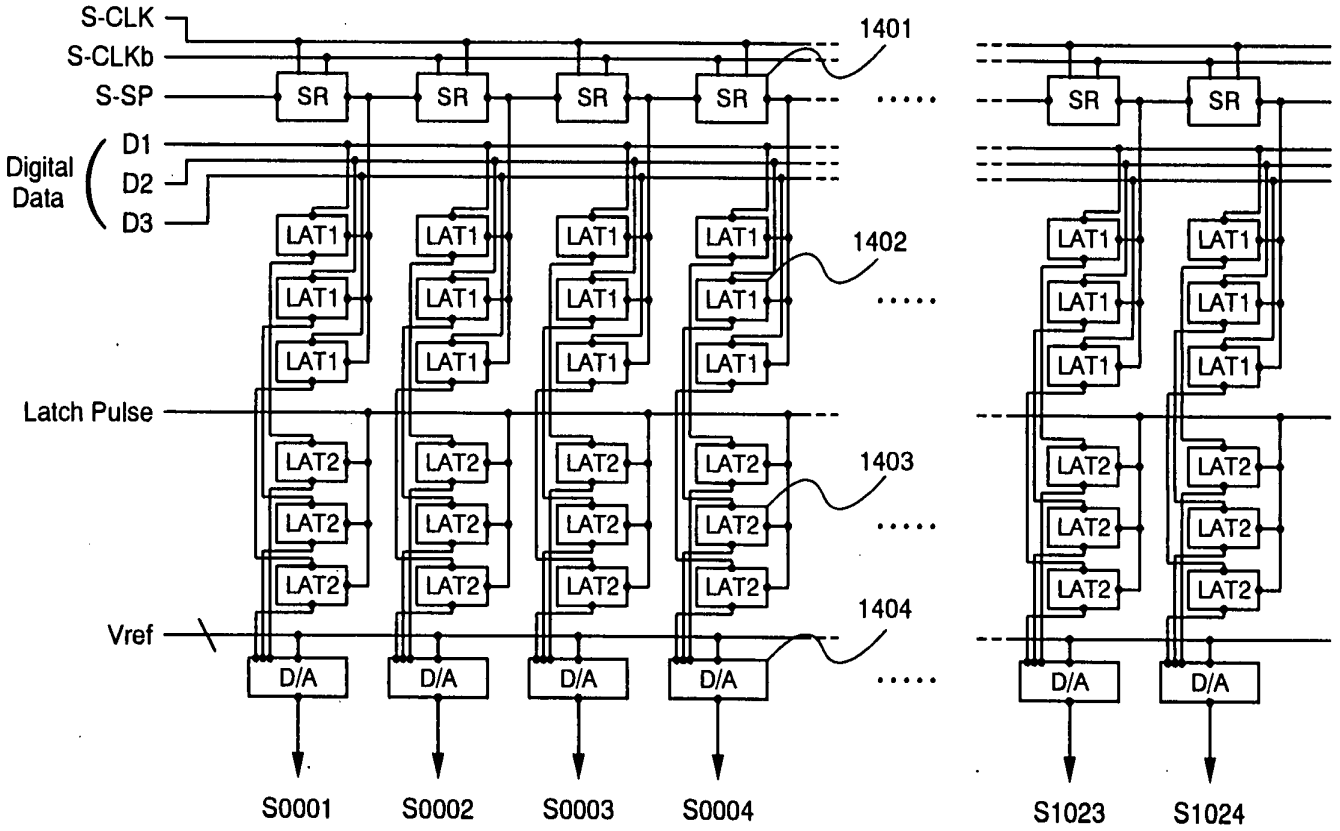


Fig. 14

Translated

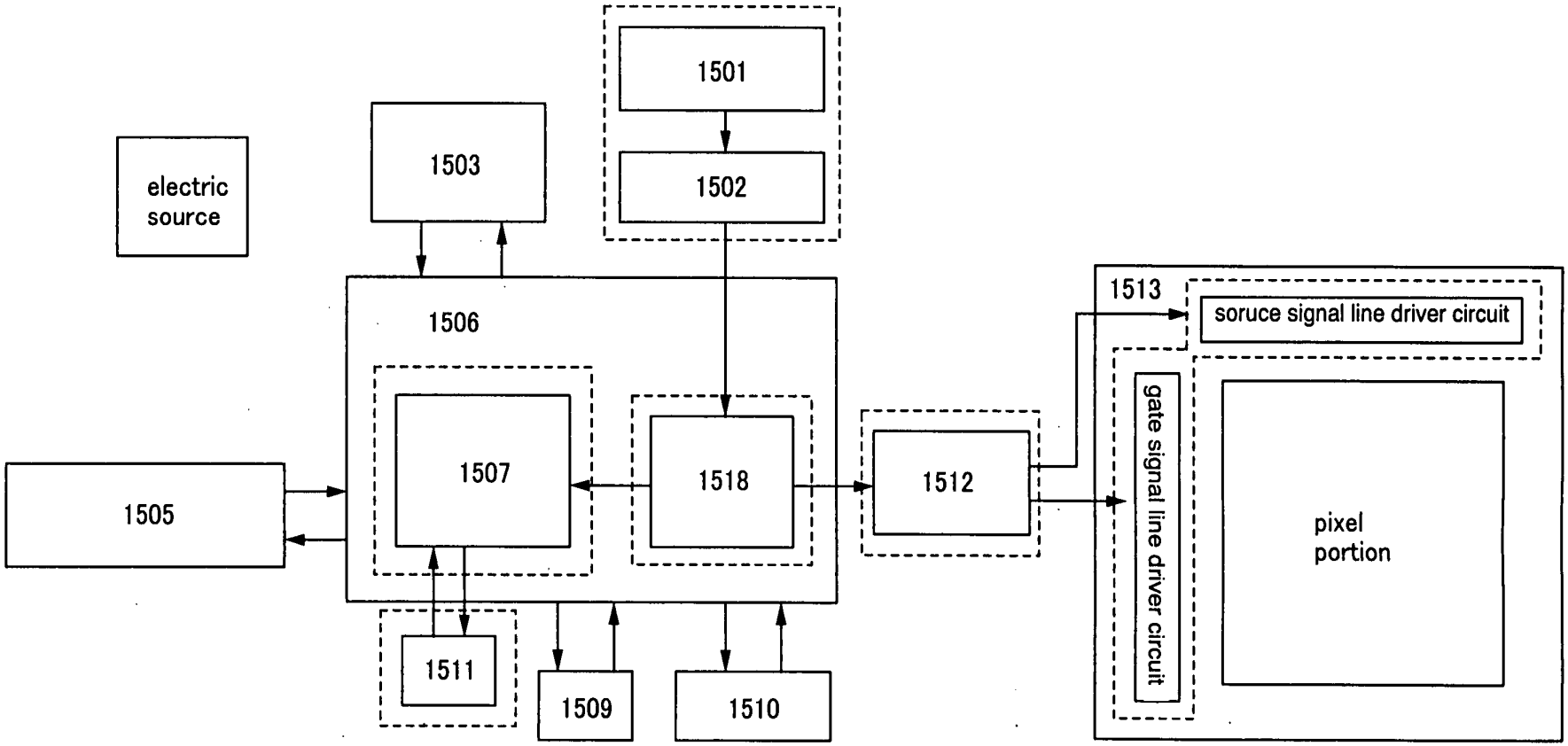


Fig. 15

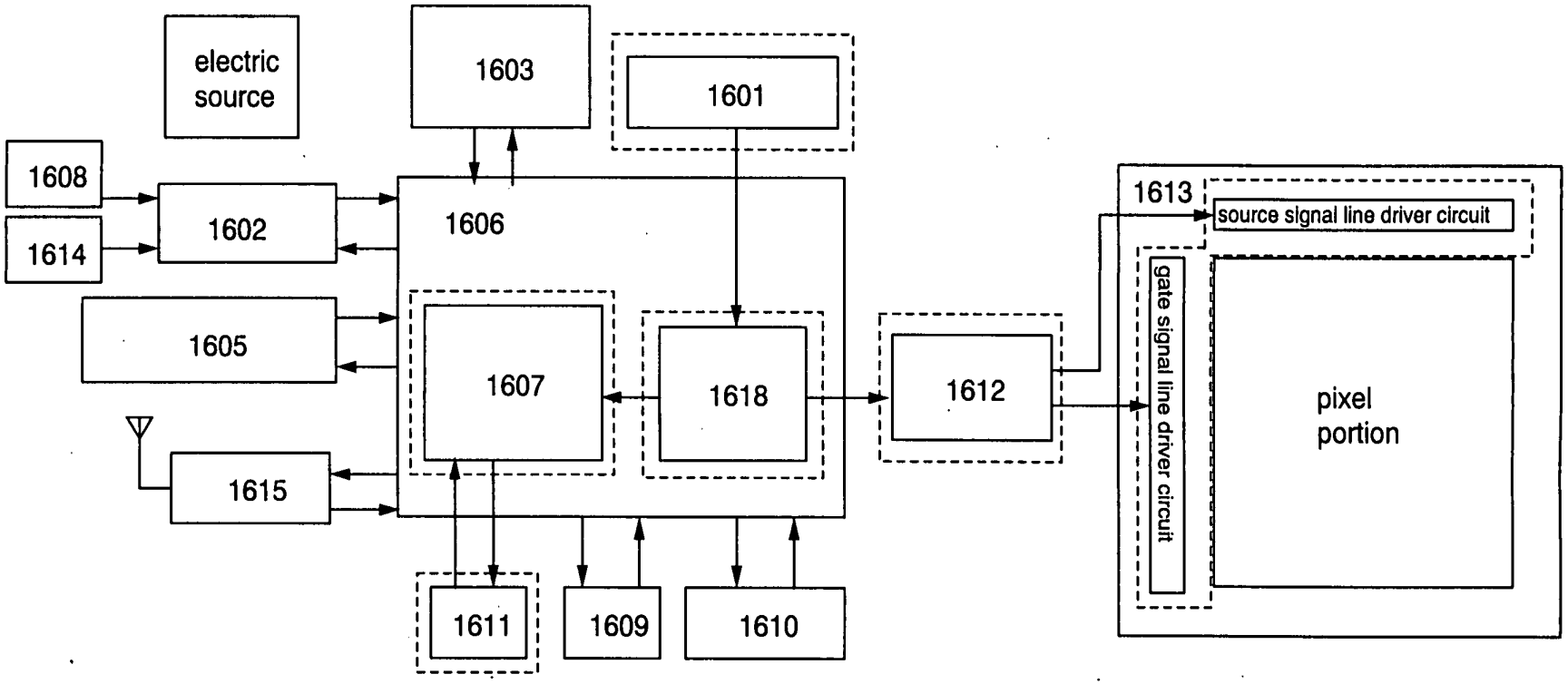

electric source
1603
1601
1608
1614
1602
1606
1605
1607
1618
1612
1615
1611
1609
1610
1613
source signal line driver circuit
gate signal line driver circuit
pixel portion

Fig. 16

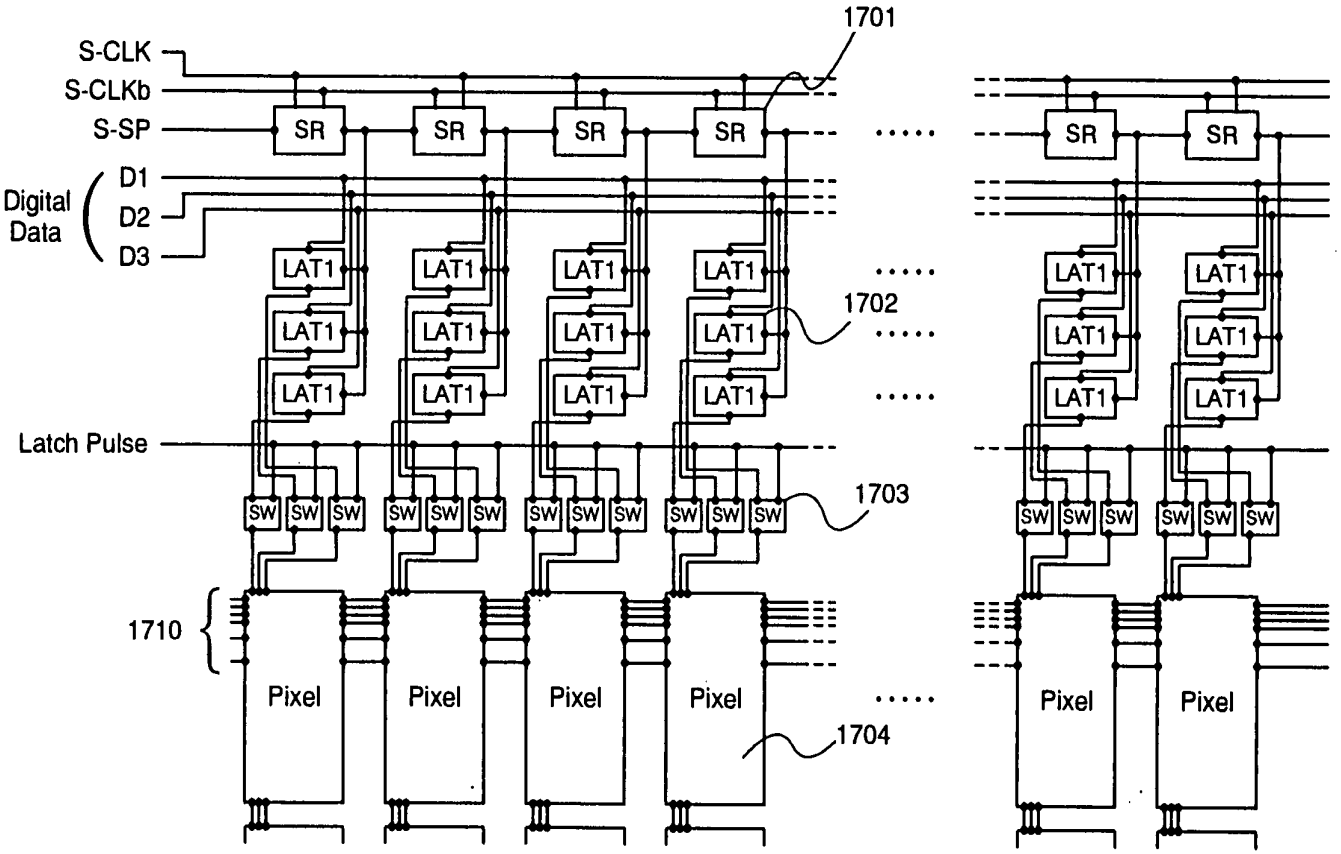

1701
S-CLK
S-CLKb
S-SP
SR
Digital Data
D1
D2
D3
LAT1
1702
Latch Pulse
1703
SW
1710
Pixel
1704

Fig. 17

TO2000-223660

Fig. 18A

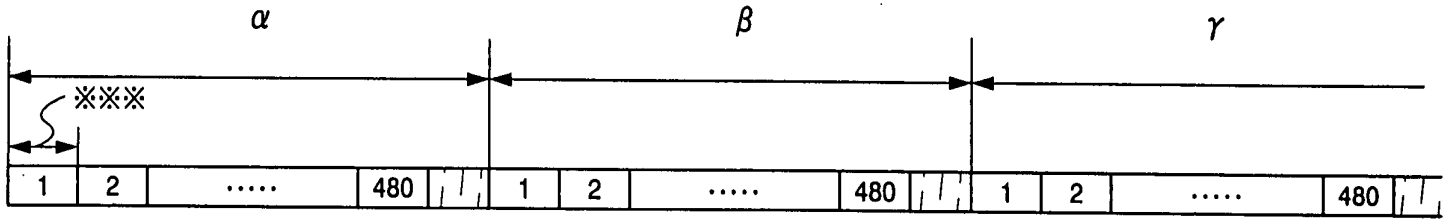


Fig. 18B

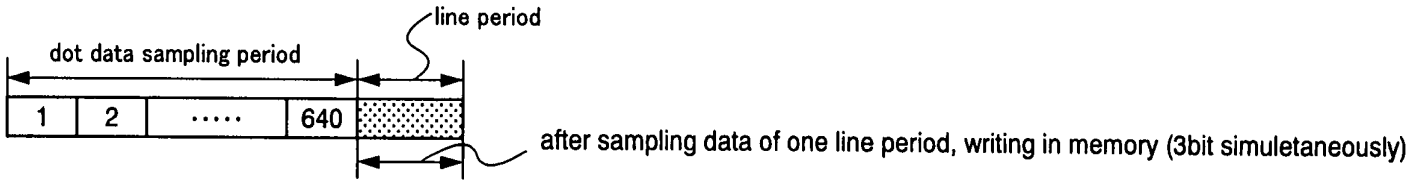


Fig. 19A

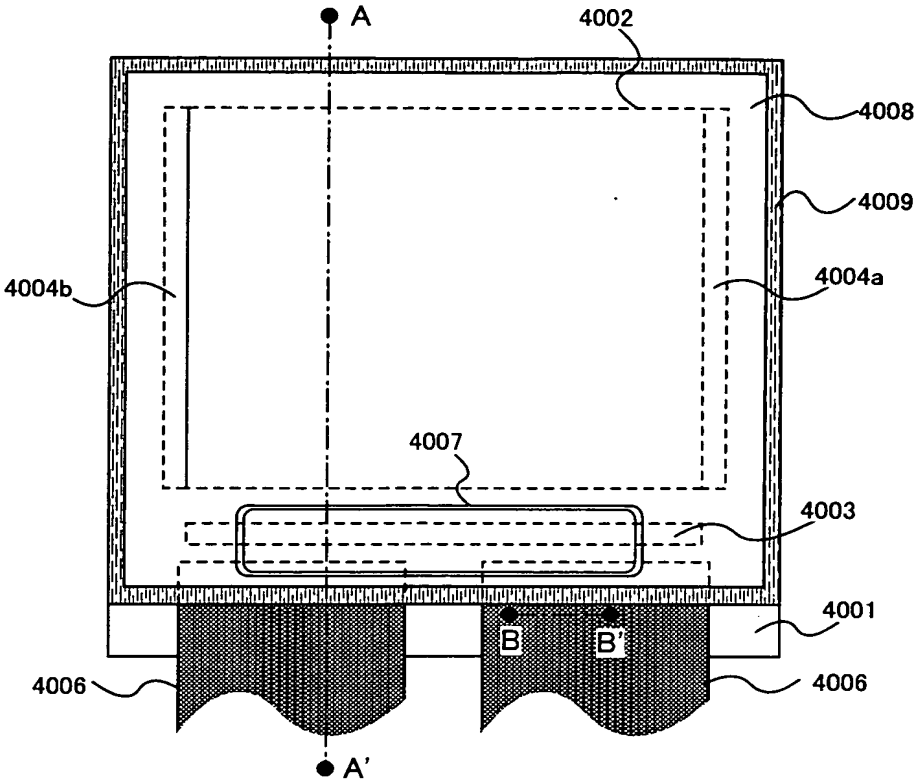


Fig. 19B

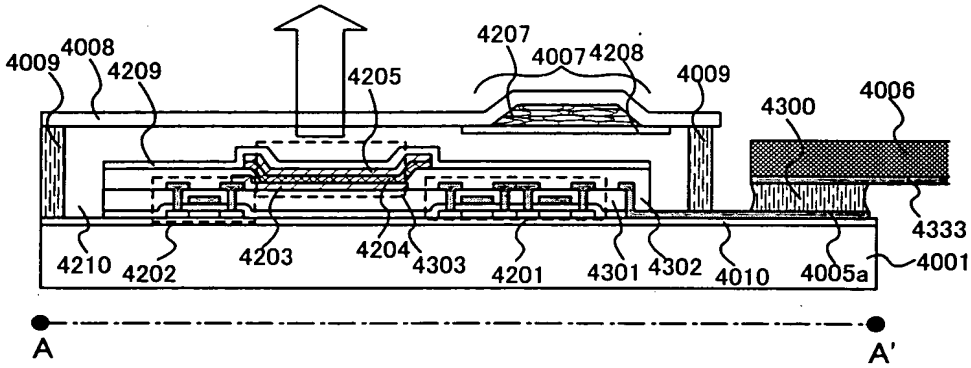
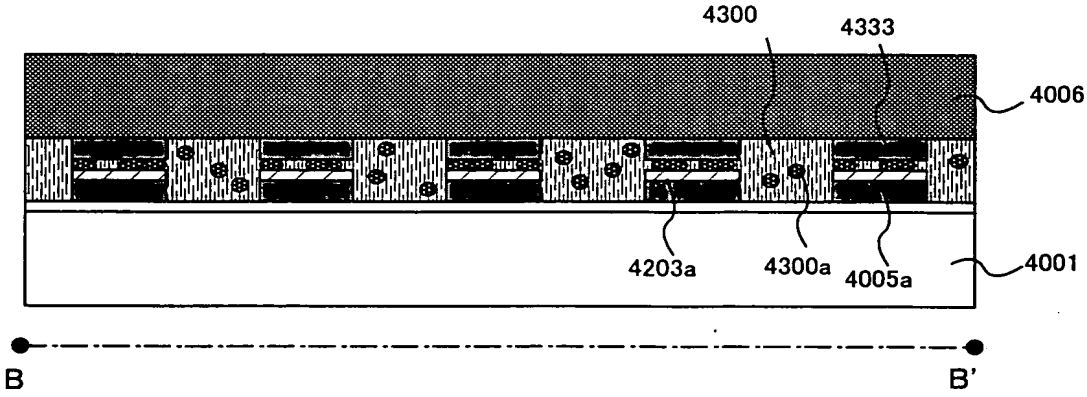


Fig. 19C



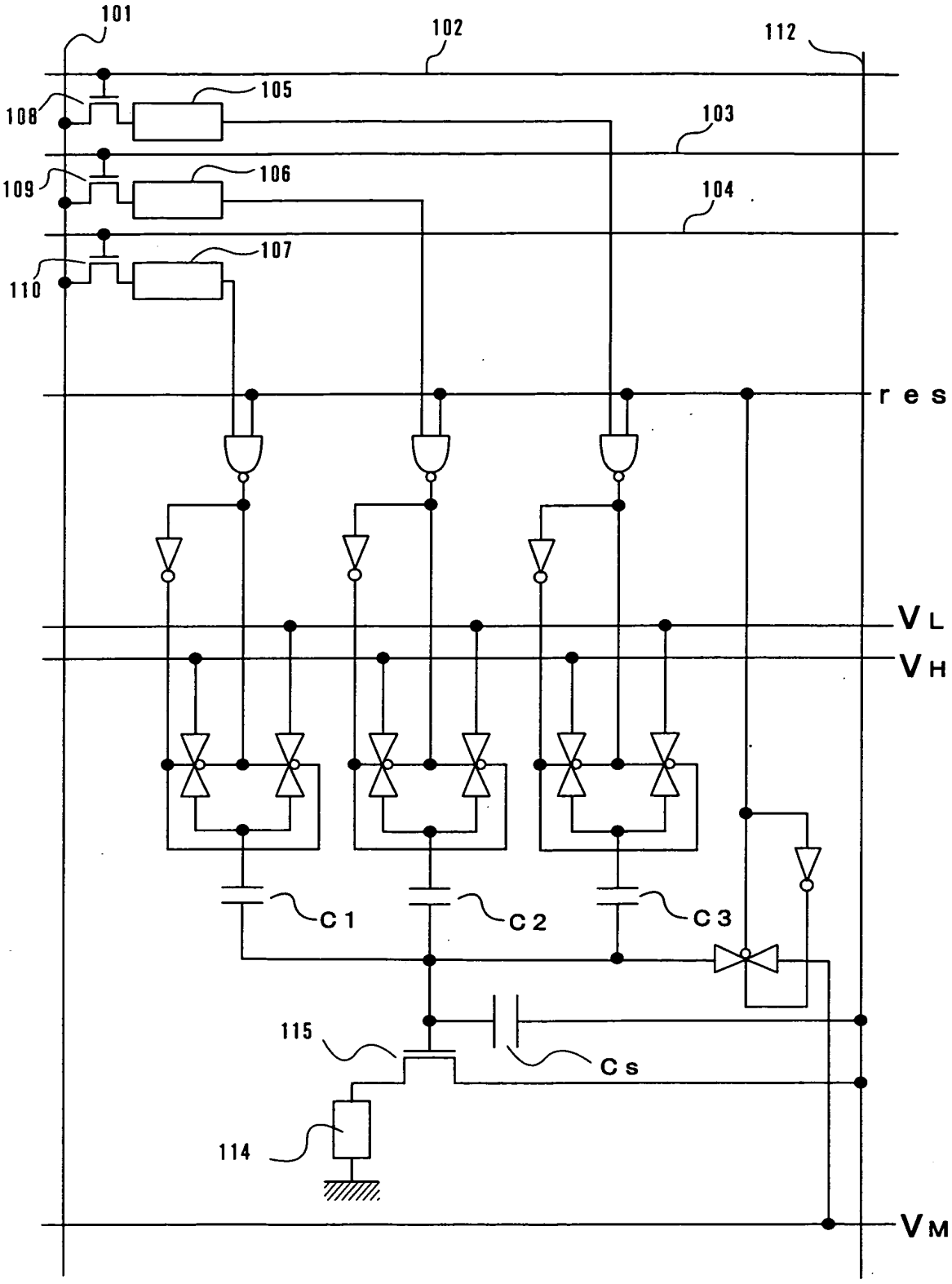

101
102
112
105
108
103
106
109
104
107
110
r e s
V L
V H
C 1
C 2
C 3
115
Cs
114
V M

Fig. 20

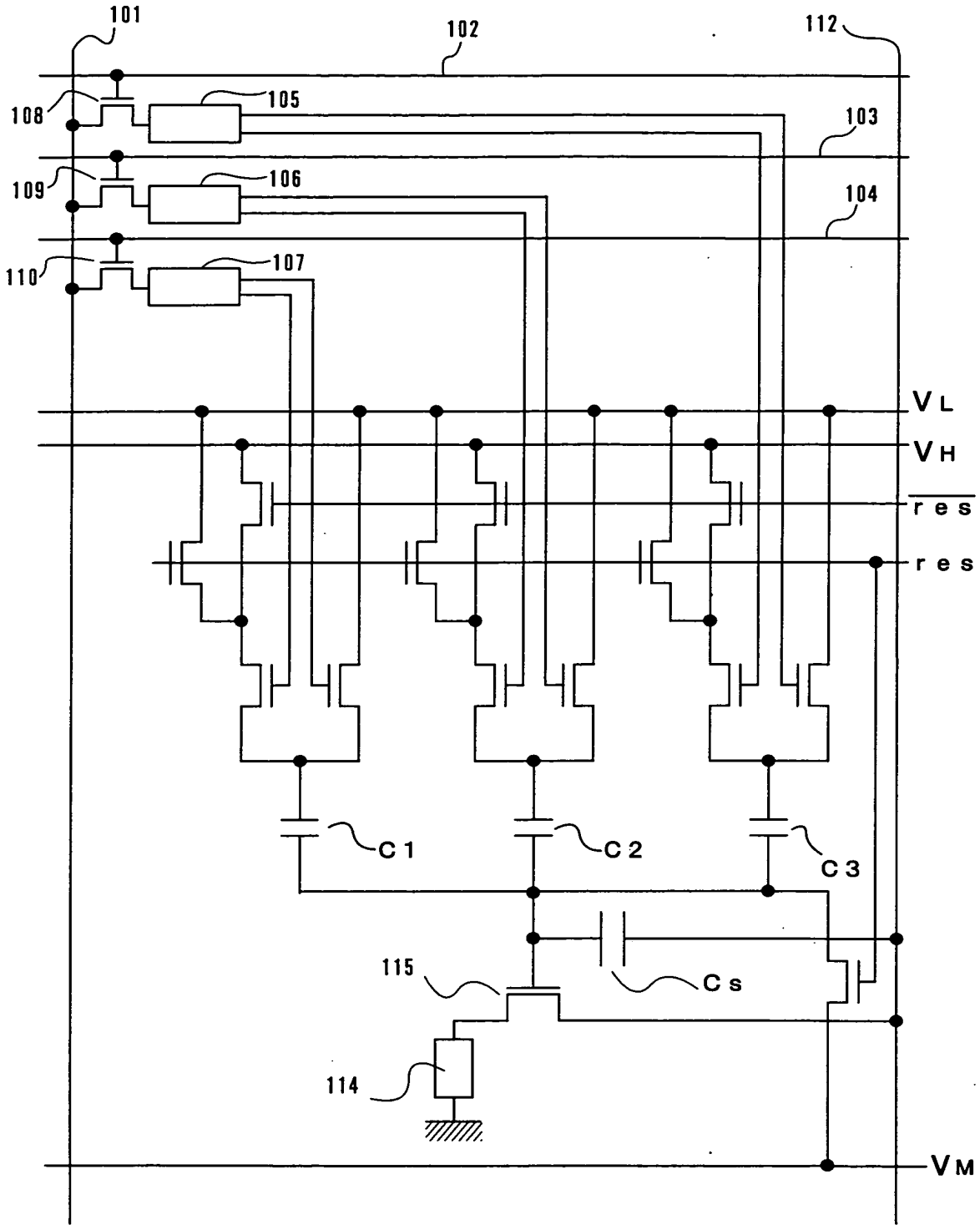

101
102
112
108
105
103
109
106
104
110
107
VL
VH
res
res
C1
C2
C3
115
Cs
114
VM

Fig. 21

TO2020 "2266T669

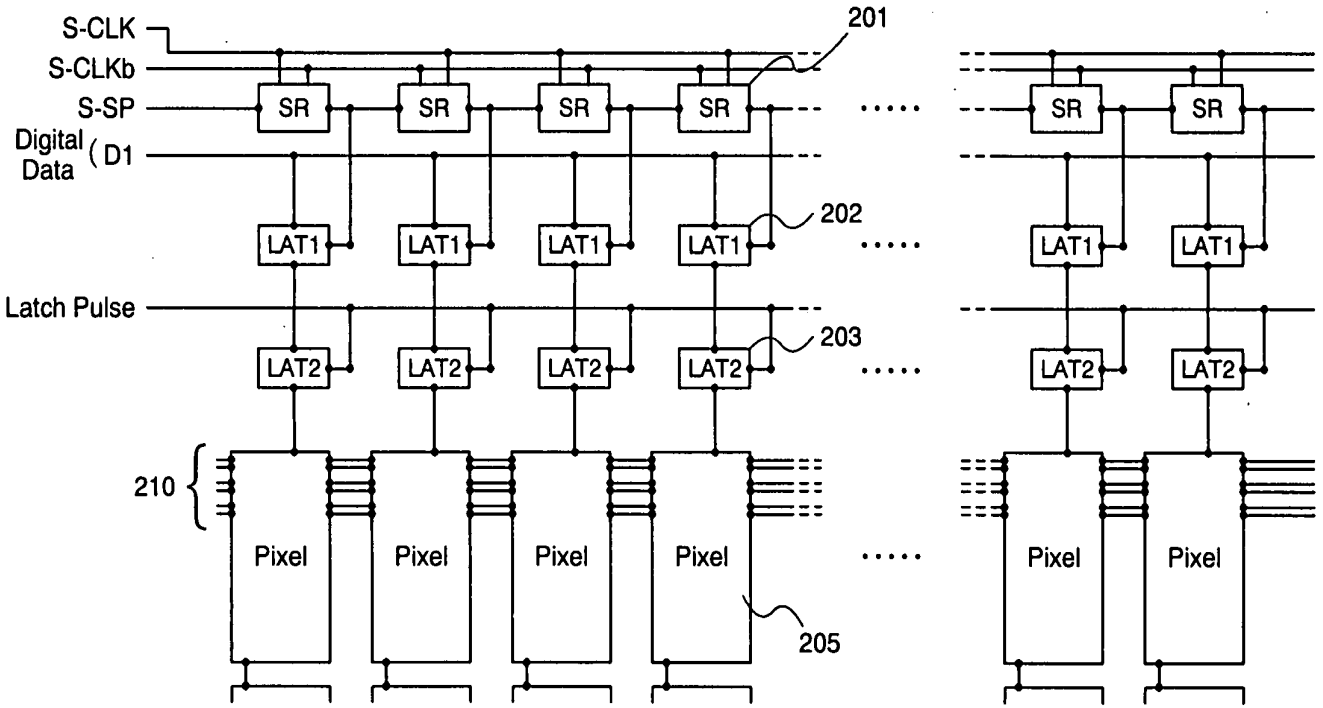


Fig. 22

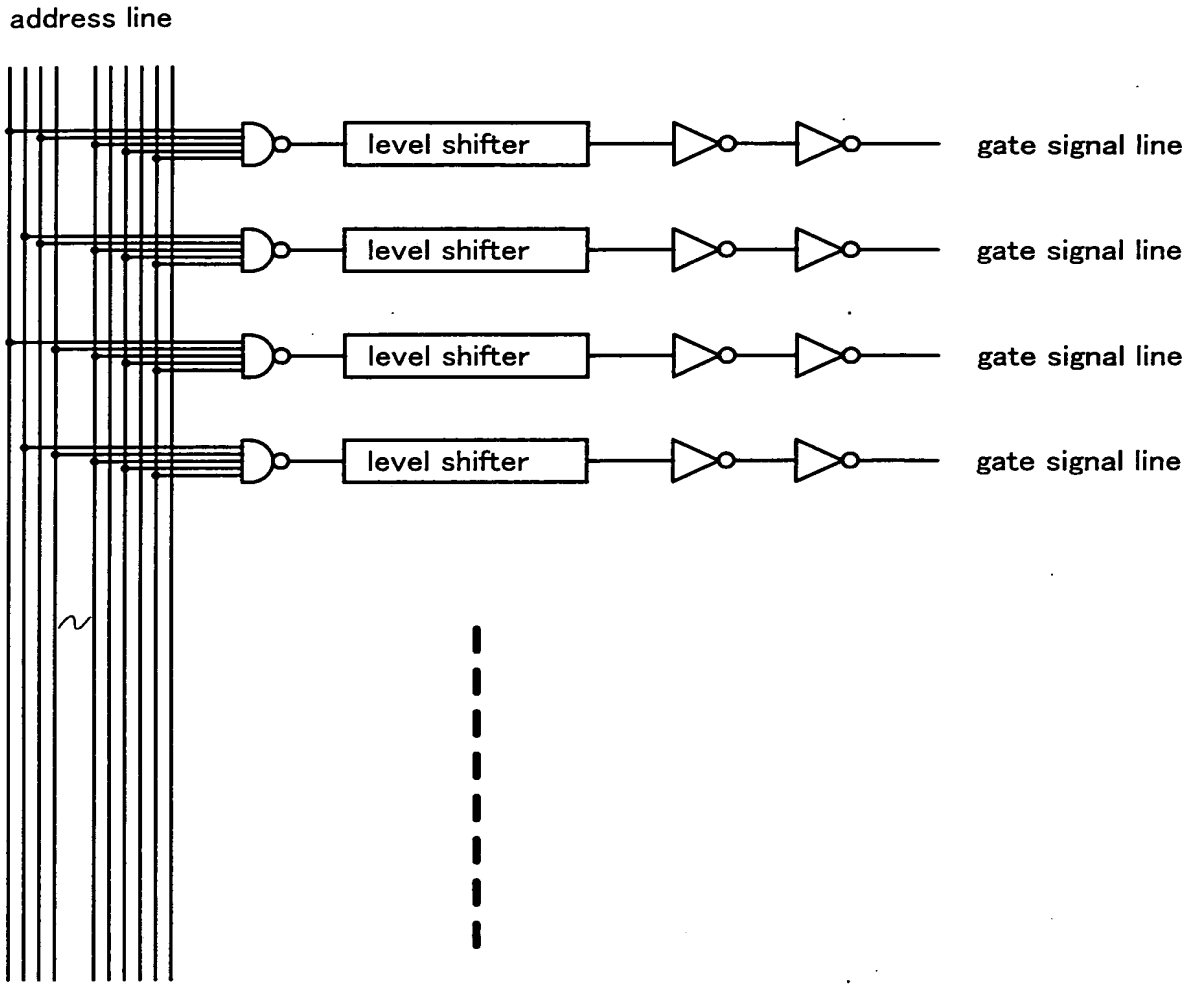

address line
level shifter
level shifter
level shifter
level shifter
gate signal line
gate signal line
gate signal line
gate signal line

Fig. 23

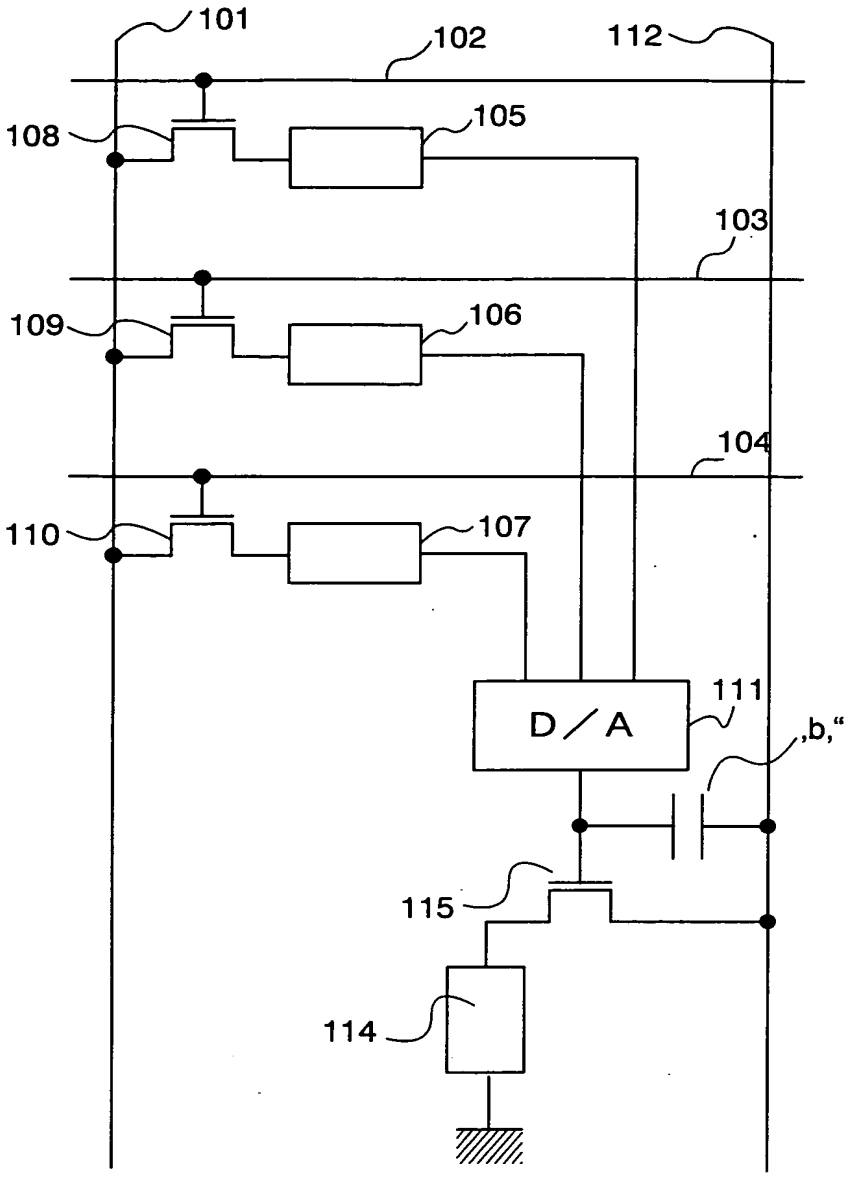


Fig. 24

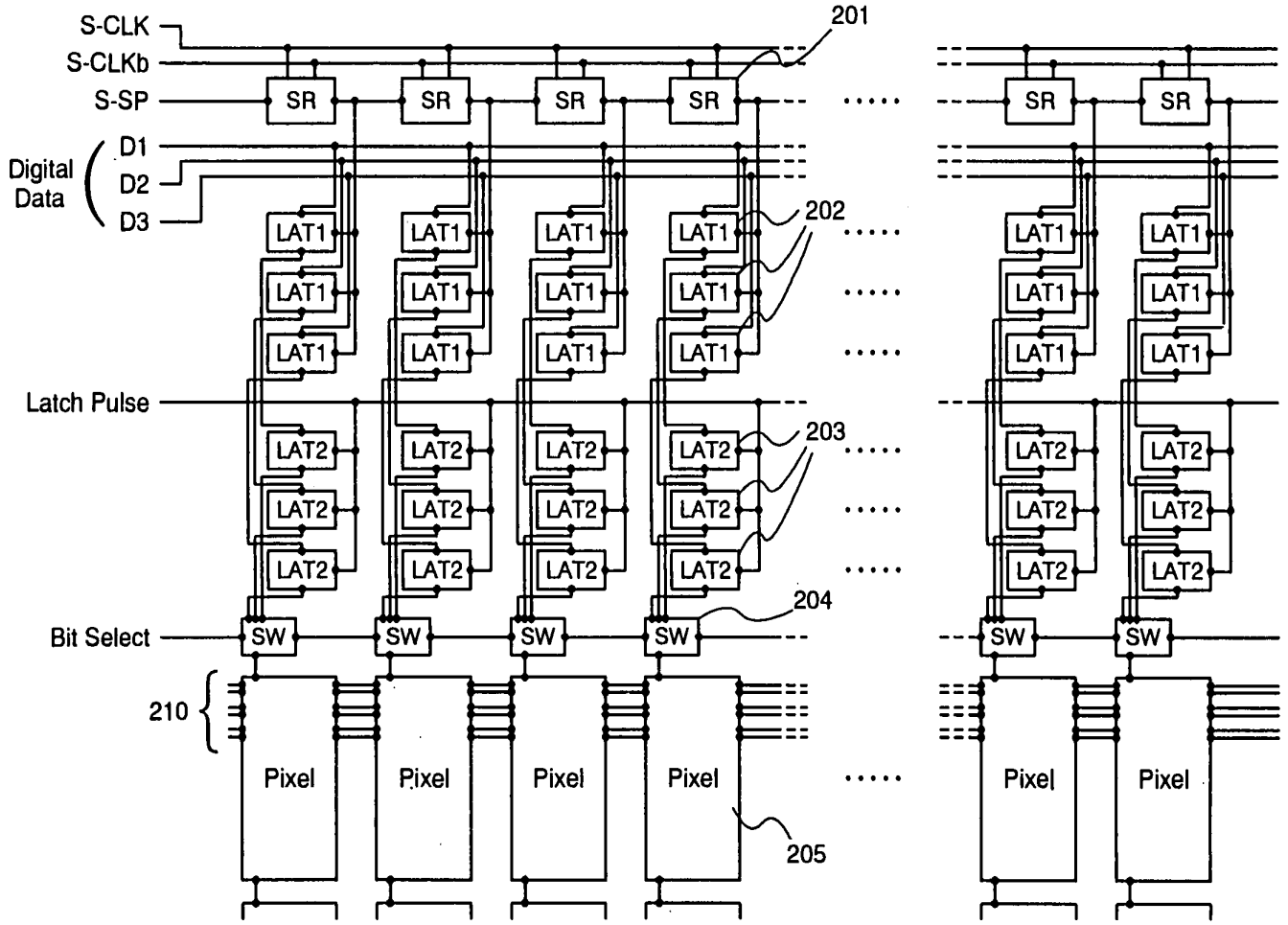

S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
Latch Pulse
Bit Select
210
SR
LAT1
LAT2
SW
Pixel
201
202
203
204
205

Fig. 25

Patent Application

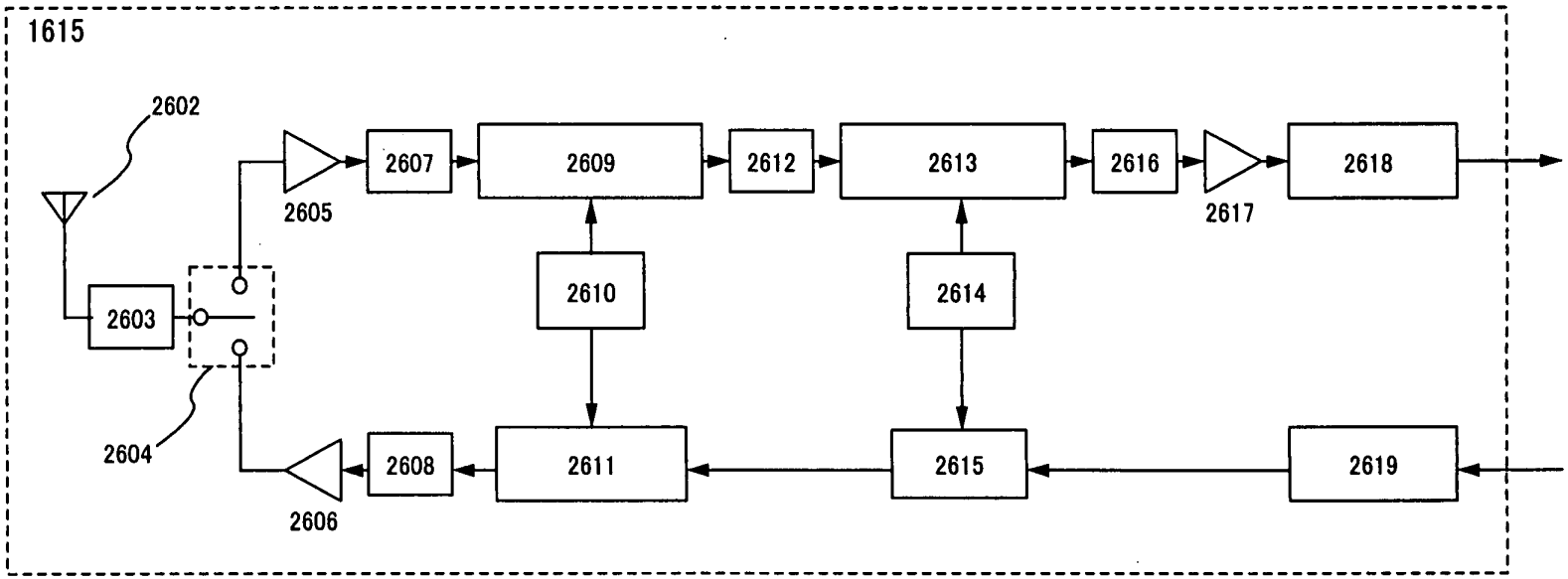


Fig. 26

Fig. 27A

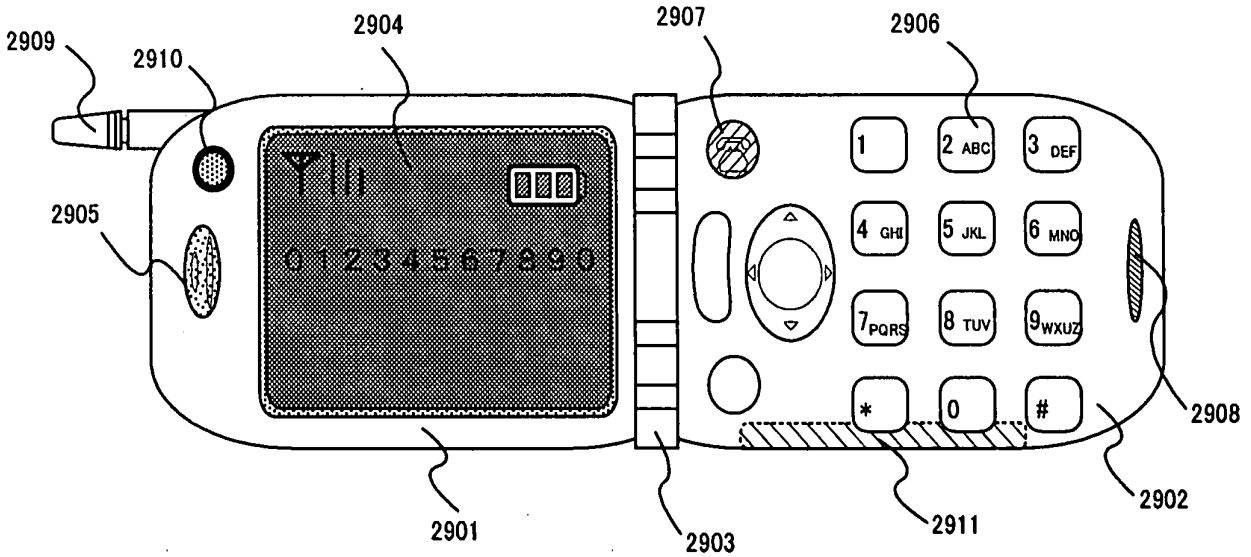
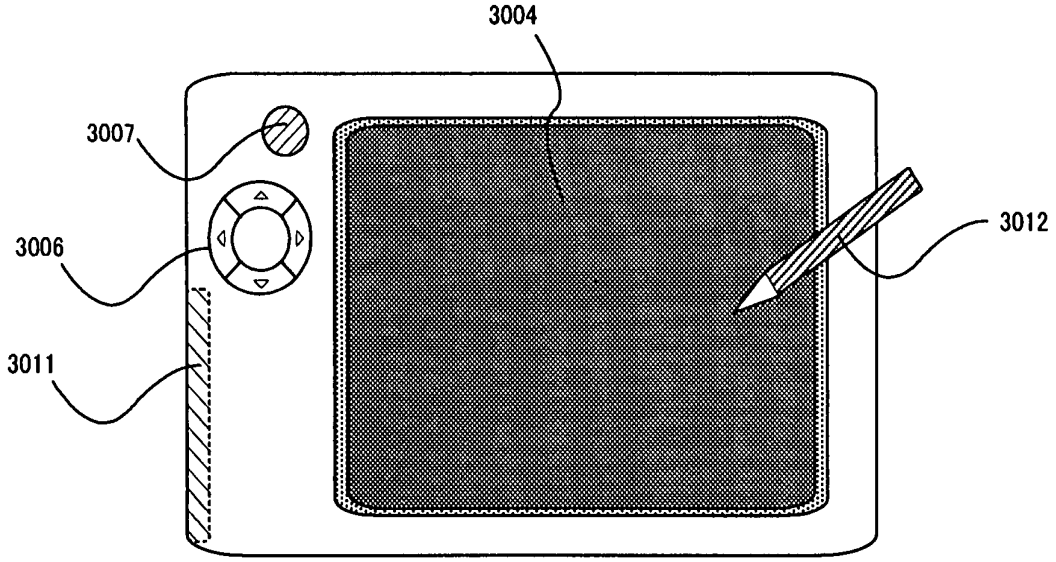


Fig. 27B



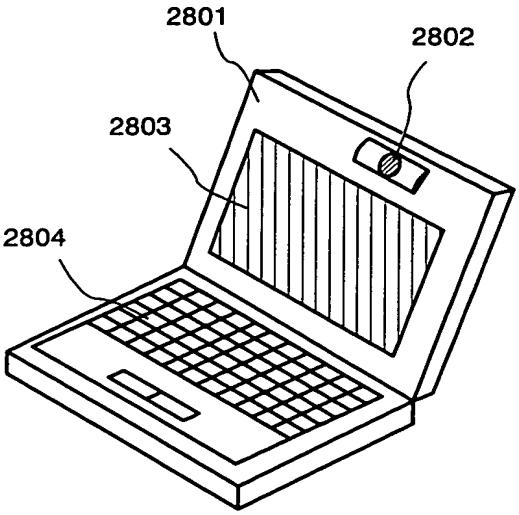


Fig. 28A

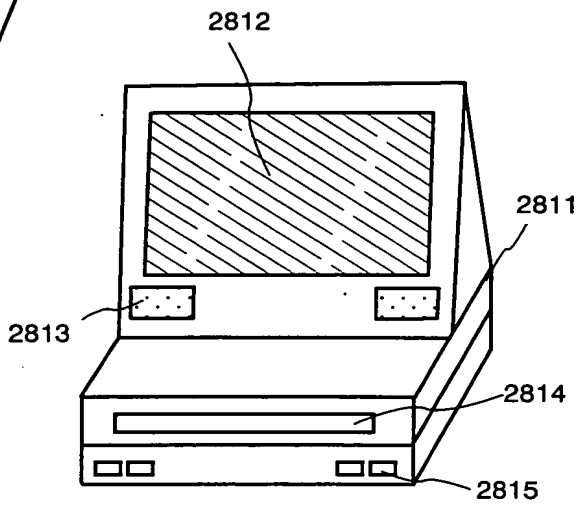


Fig. 28B

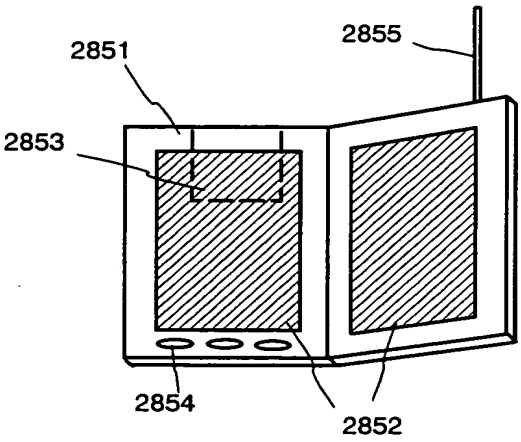


Fig. 28C

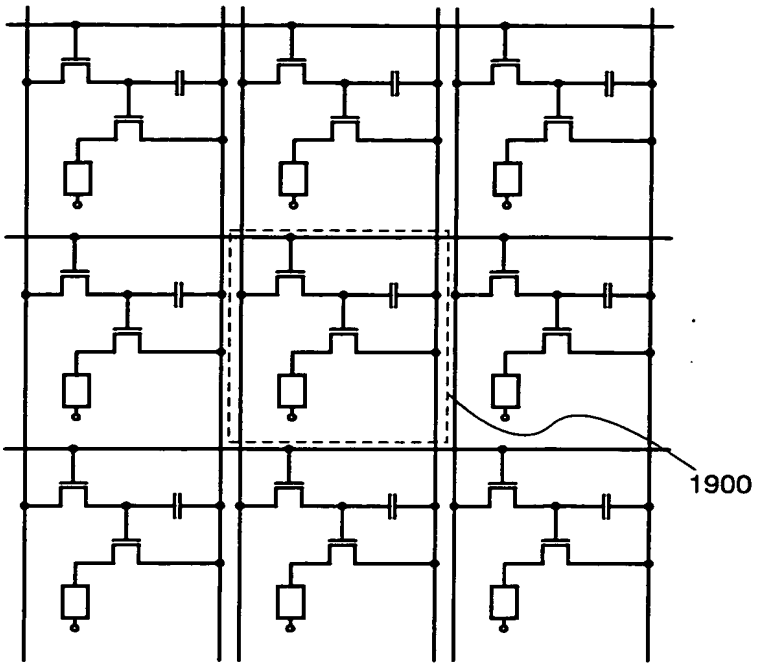


Fig. 29A

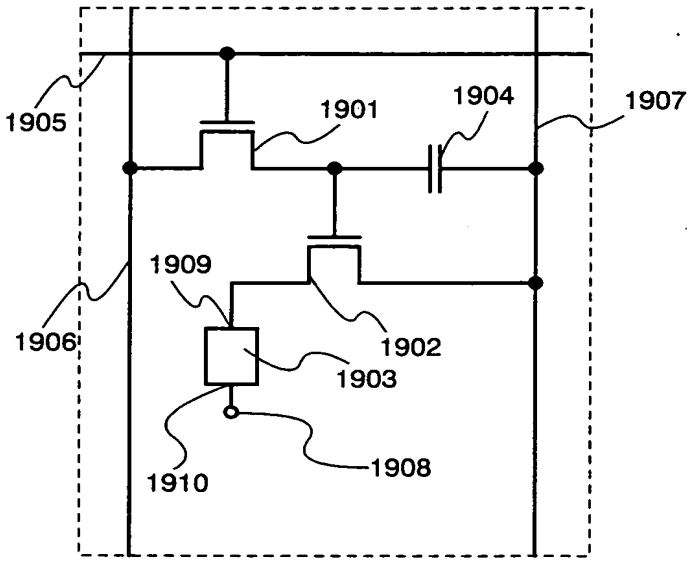


Fig. 29B

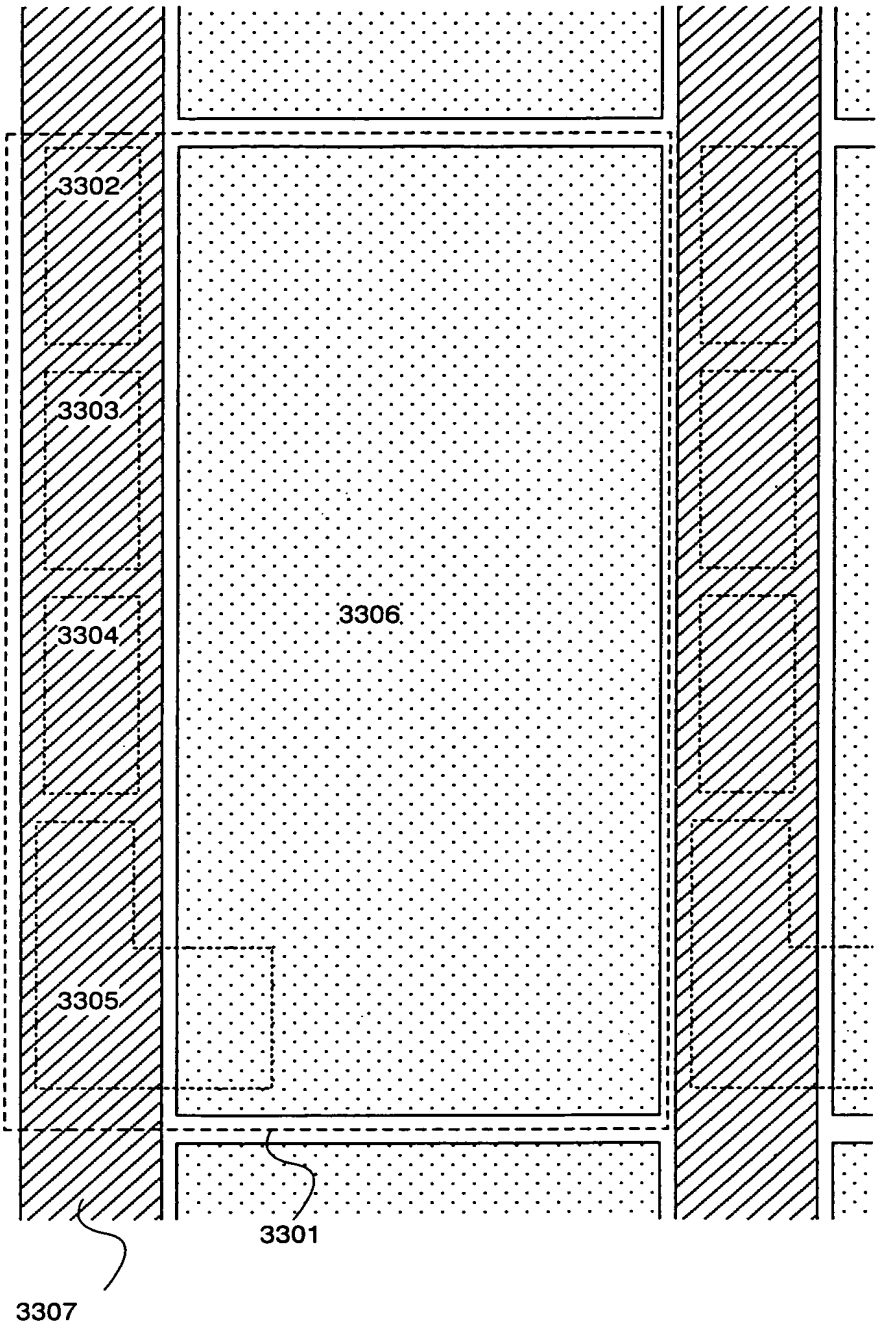


Fig. 30

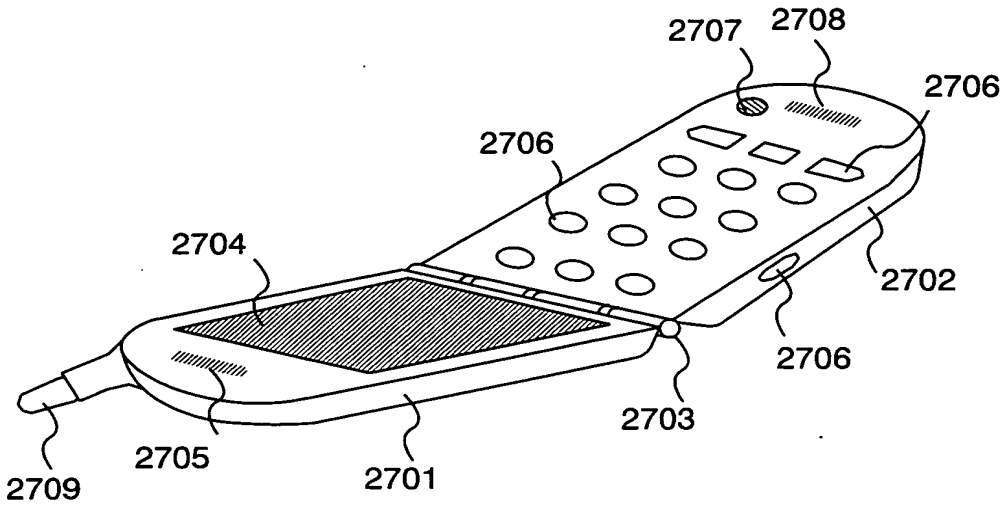


Fig. 31

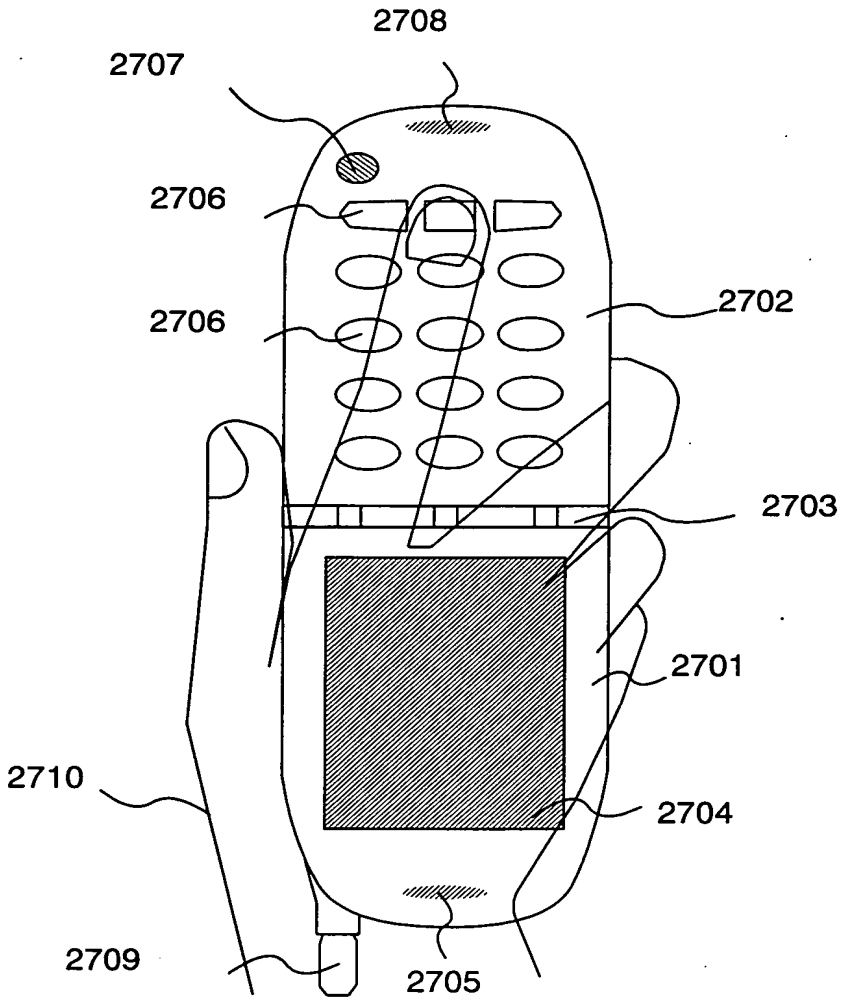


Fig. 32

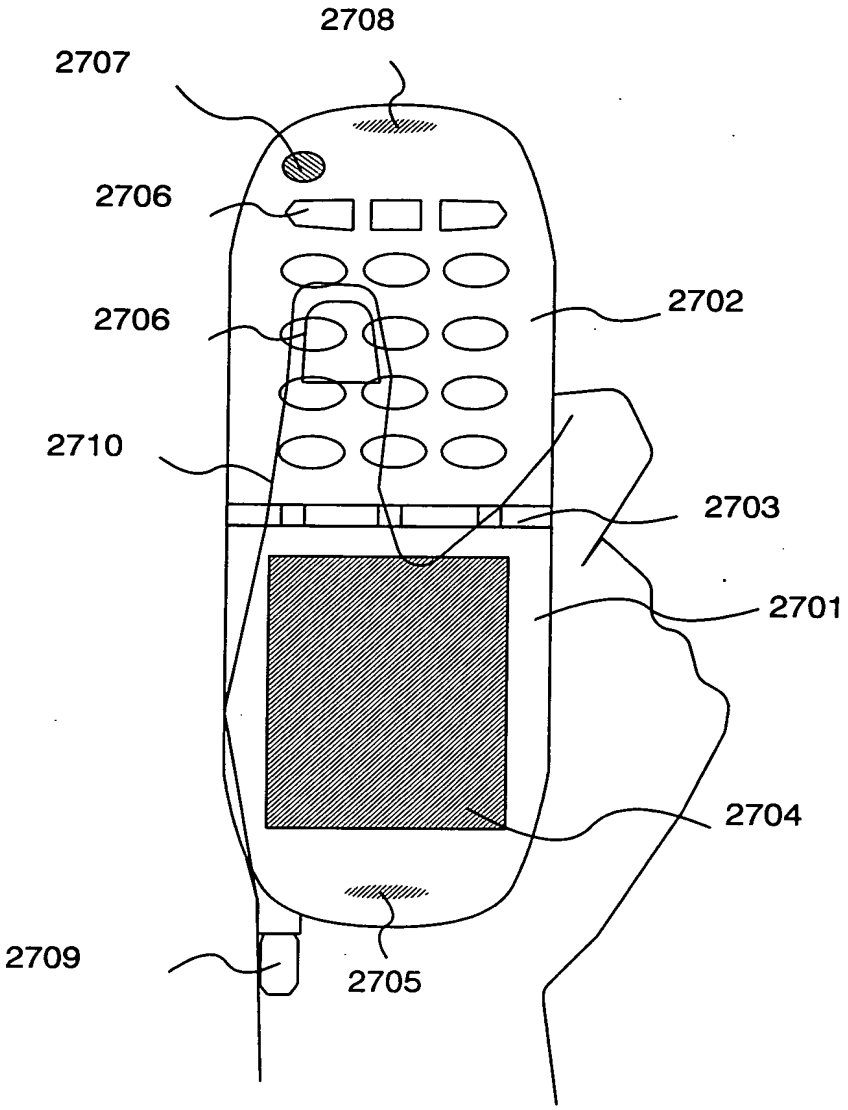


Fig. 33

driving waveform →

optical response waveform →

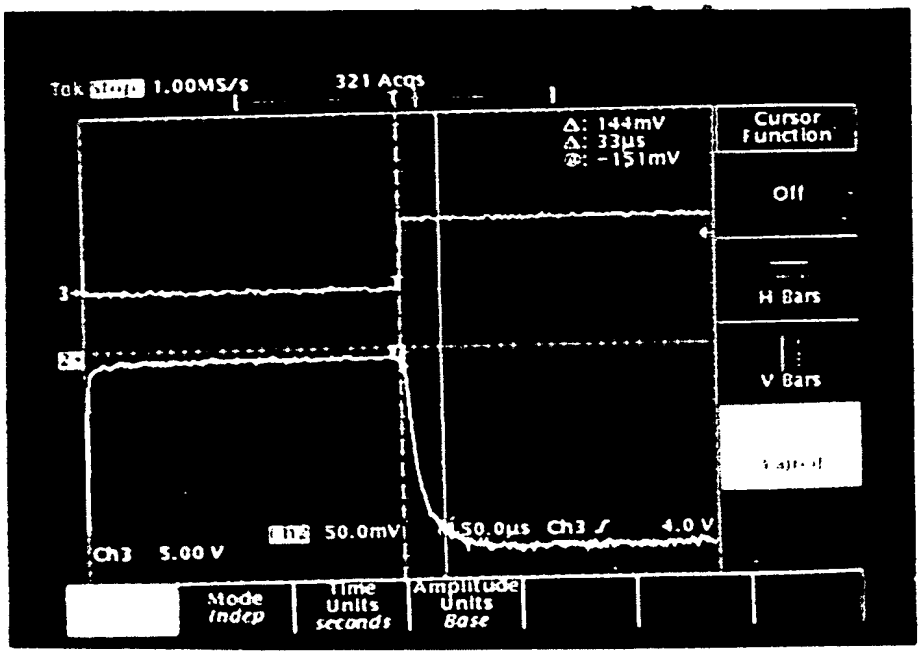


Fig. 34